

FIG. 1  
(PRIOR ART)

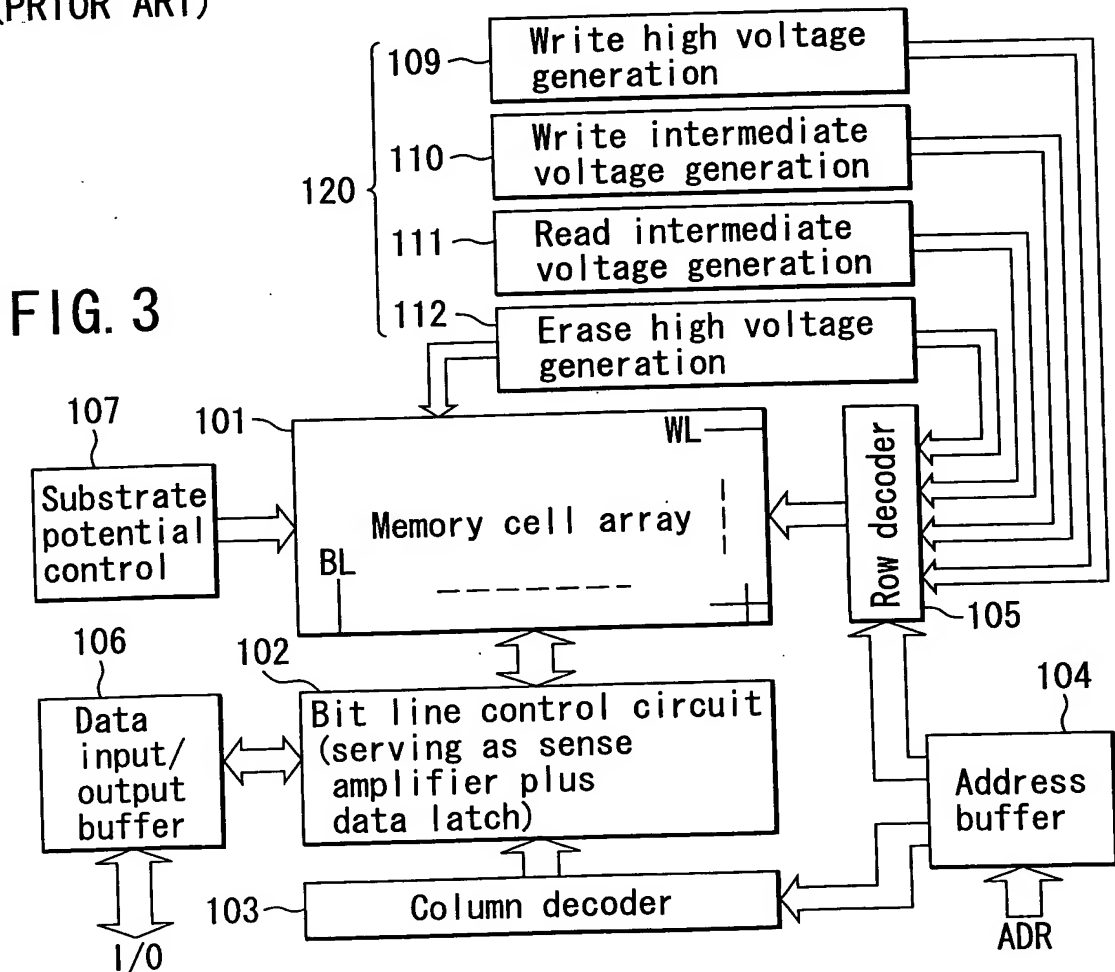
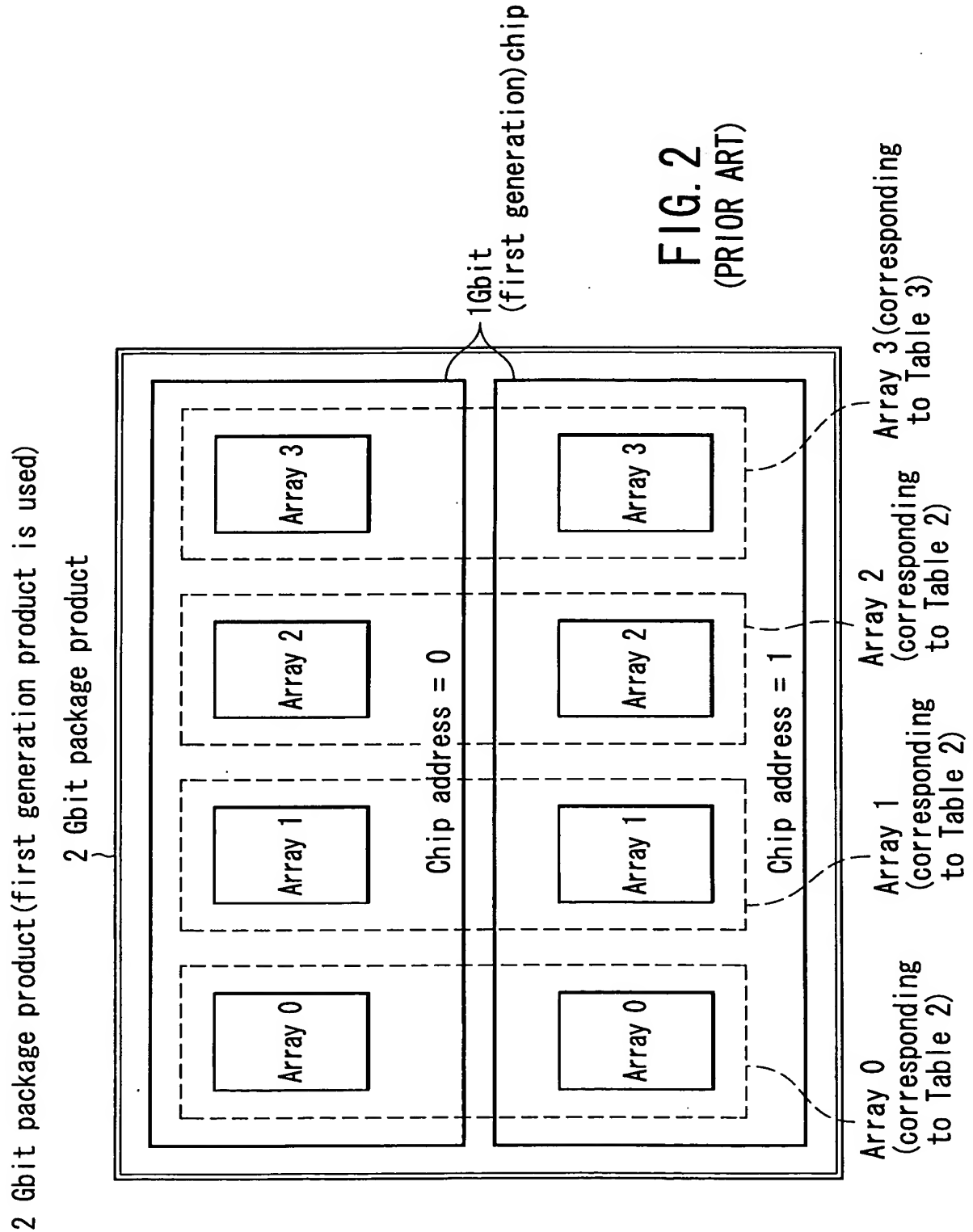


FIG. 3



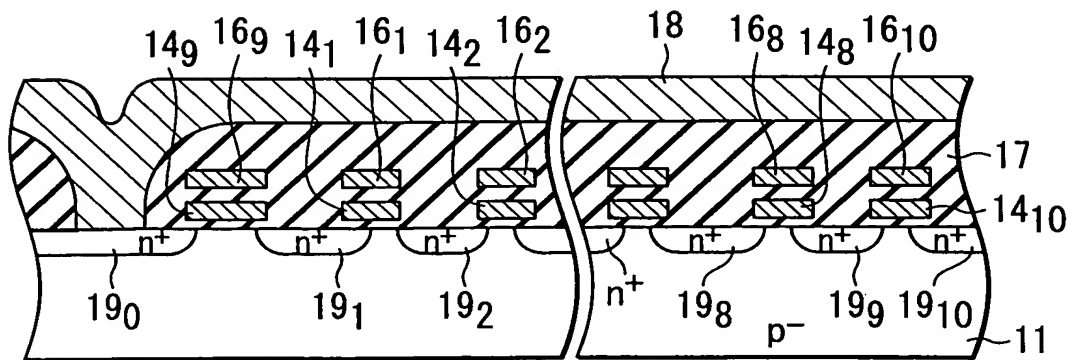
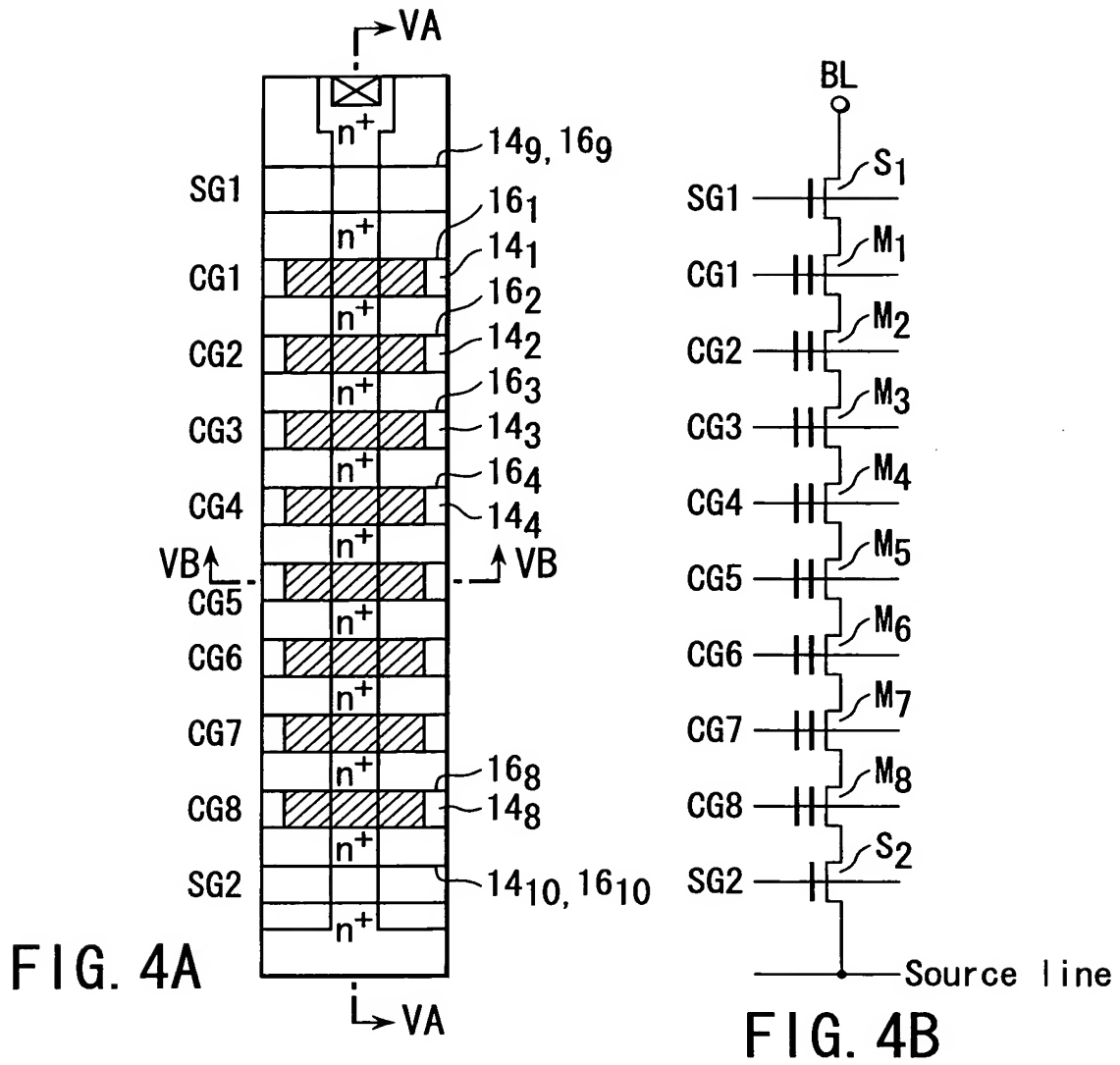
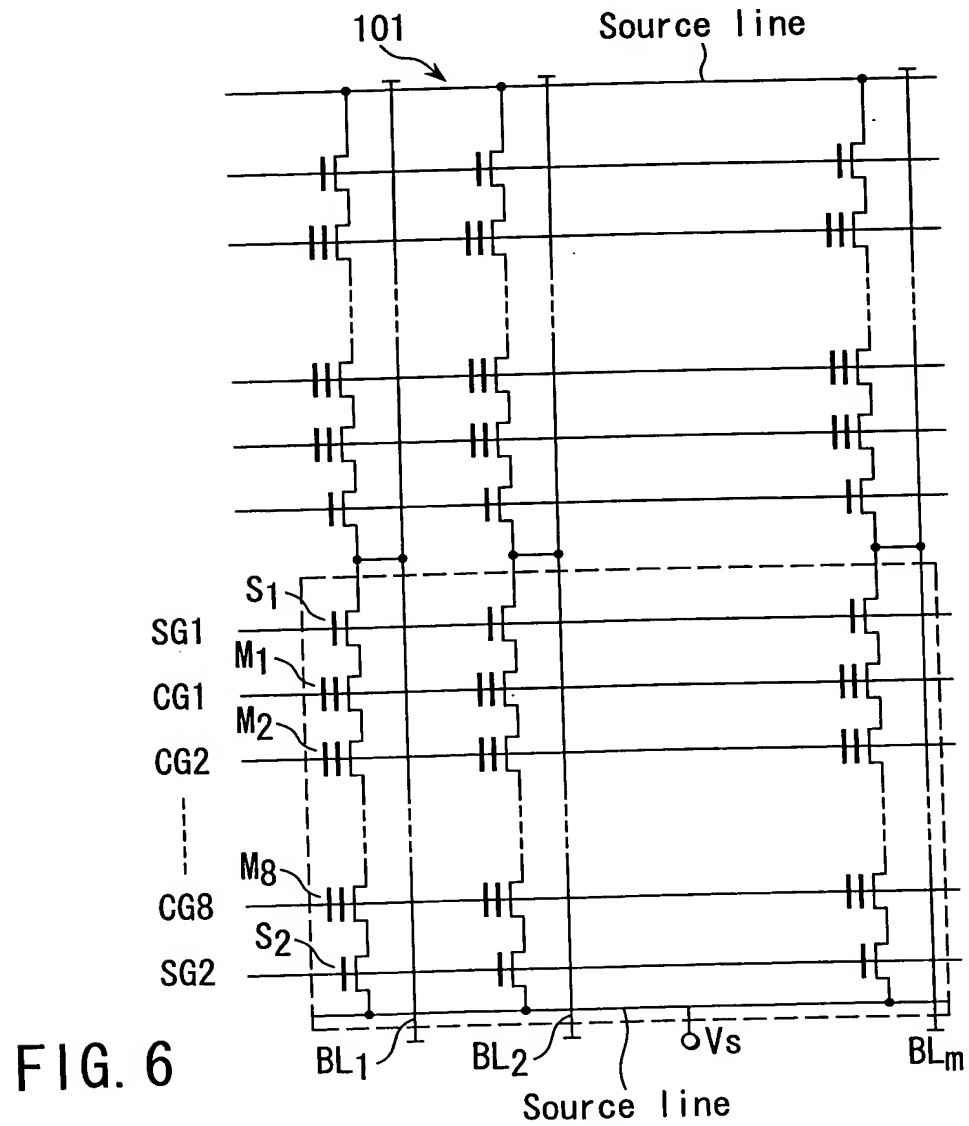
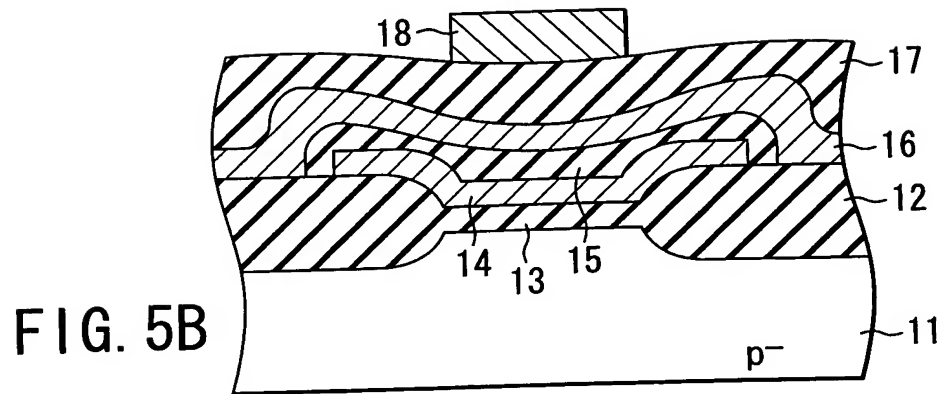


FIG. 5A



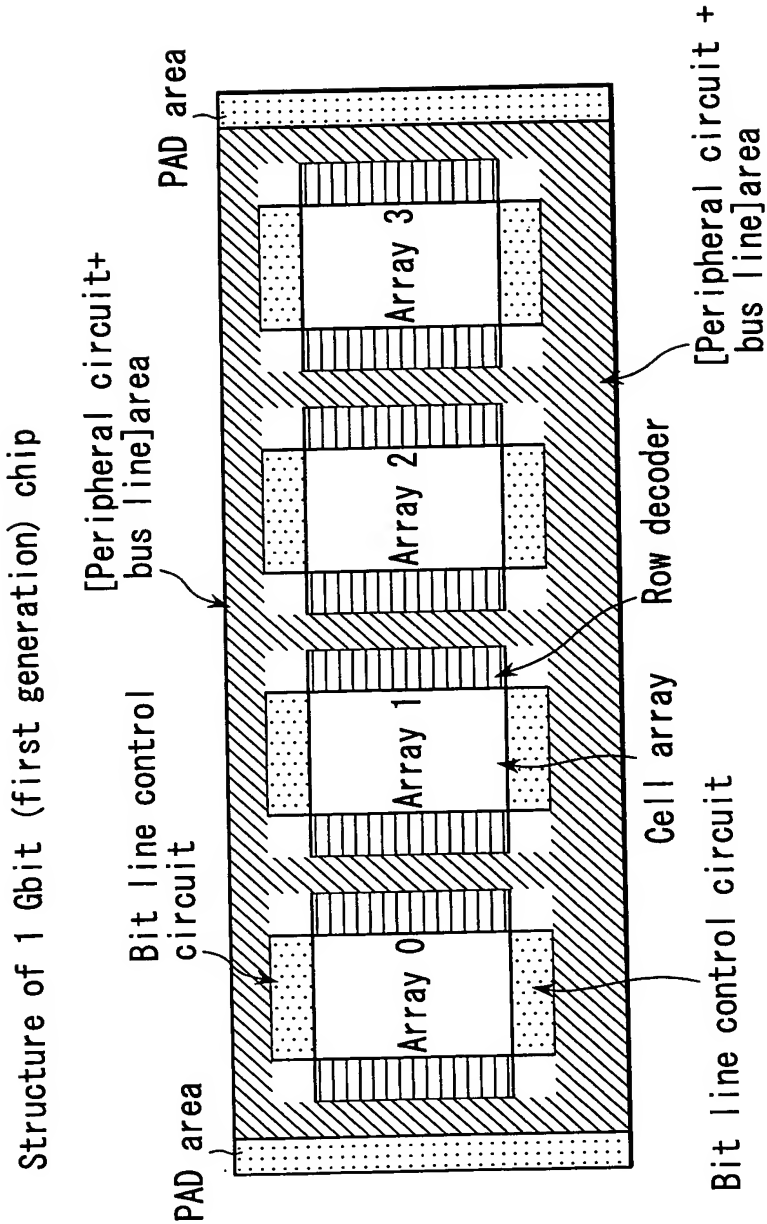


FIG. 7

Chip image when package product of FIG. 15 is seen from external device

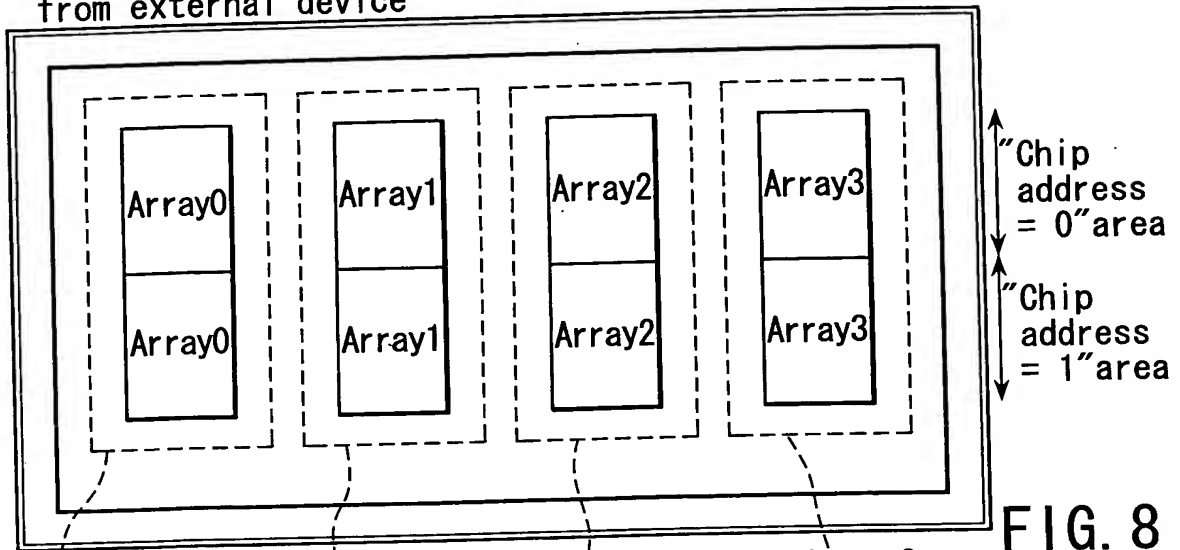


FIG. 8

Array 0 (corresponding to Table 2)    Array 1 (corresponding to Table 2)    Array 2 (corresponding to Table 2)    Array 3 (corresponding to Table 2)

2 Gbit package product  
(second generation product is used)

2 Gbit package product

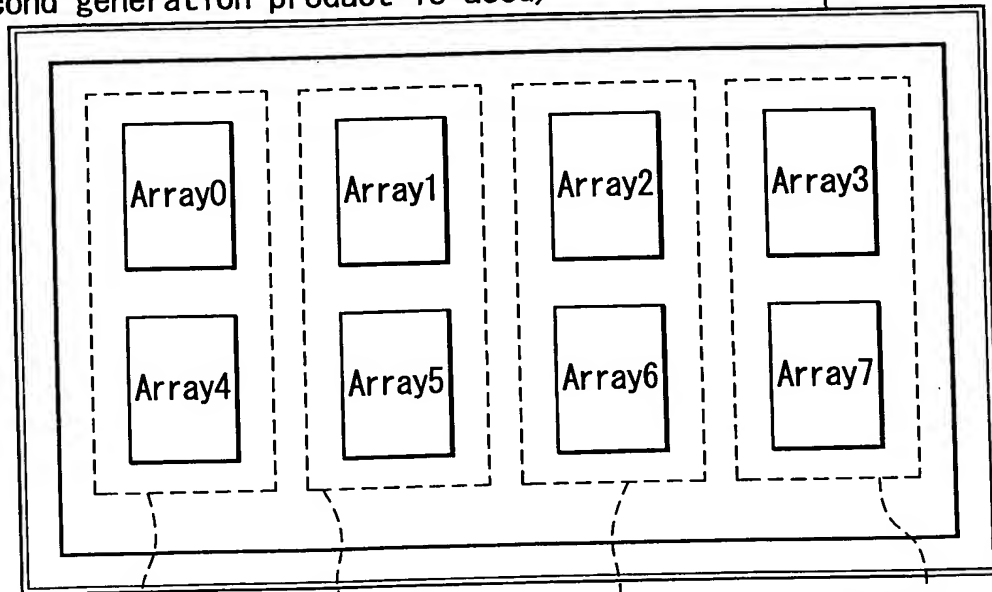


FIG. 9

Array 0 (corresponding to Table 4)    Array 1 (corresponding to Table 4)    Array 2 (corresponding to Table 4)    Array 3 (corresponding to Table 4)

4 Gbit package product (first generation product is used)  
4 Gbit package product      1 Gbit (first generation) chip

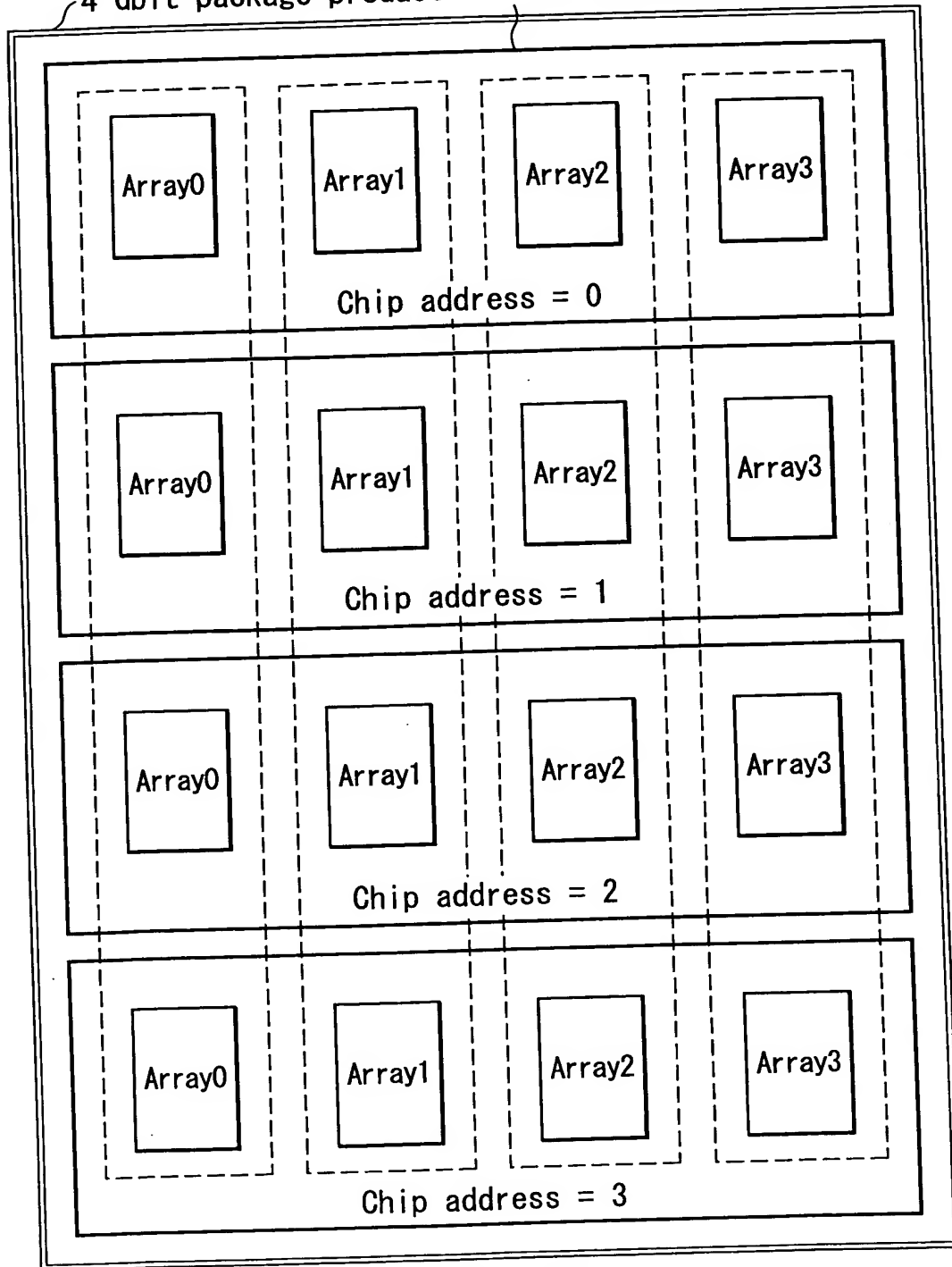


FIG. 10

Gbit package product  
(second generation product is used)

4 Gbit package product

2 Gbit(second generation) chip

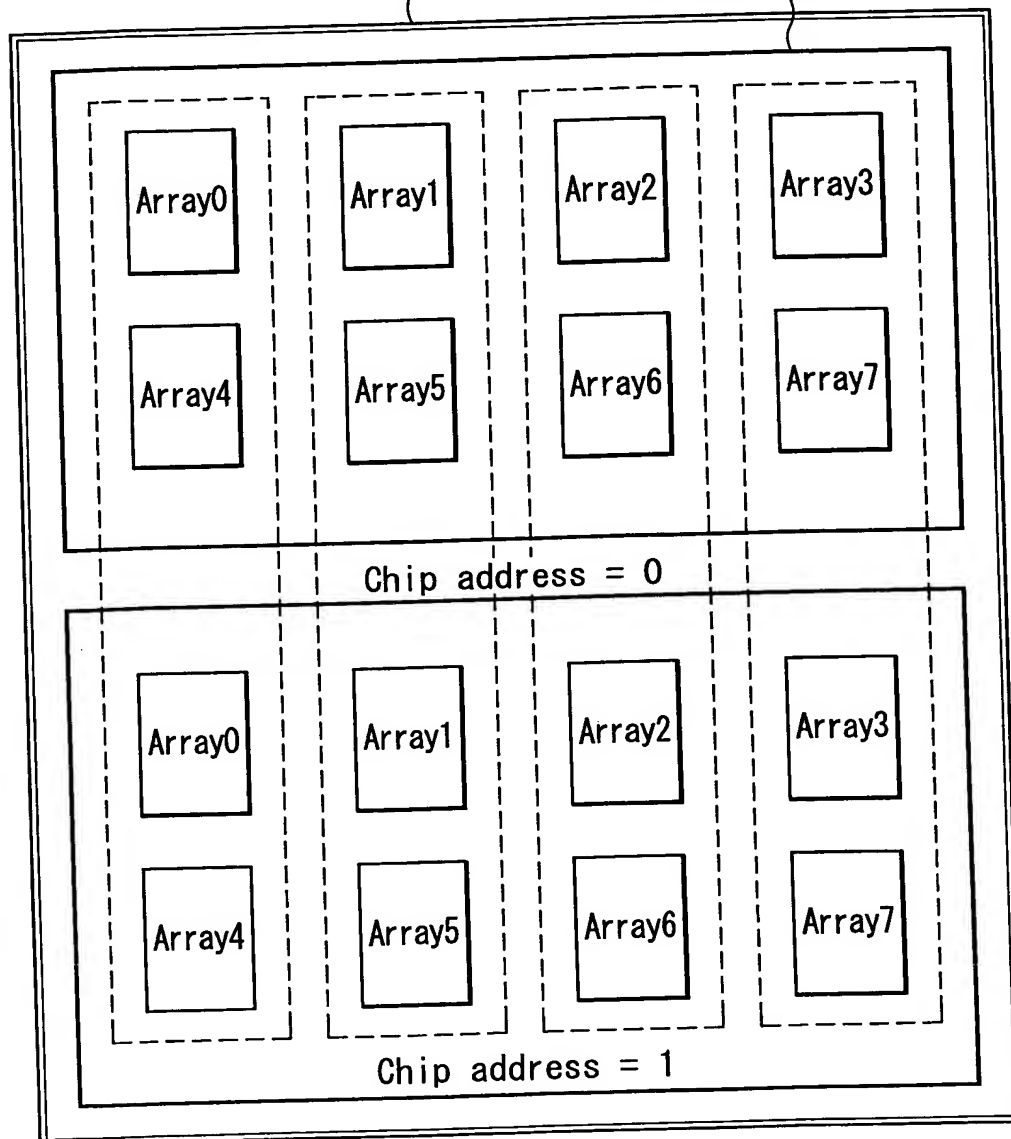


FIG. 11

4 Gbit package product  
(third generation product is used)

4 Gbit package product  
4 Gbit (third generation) chip

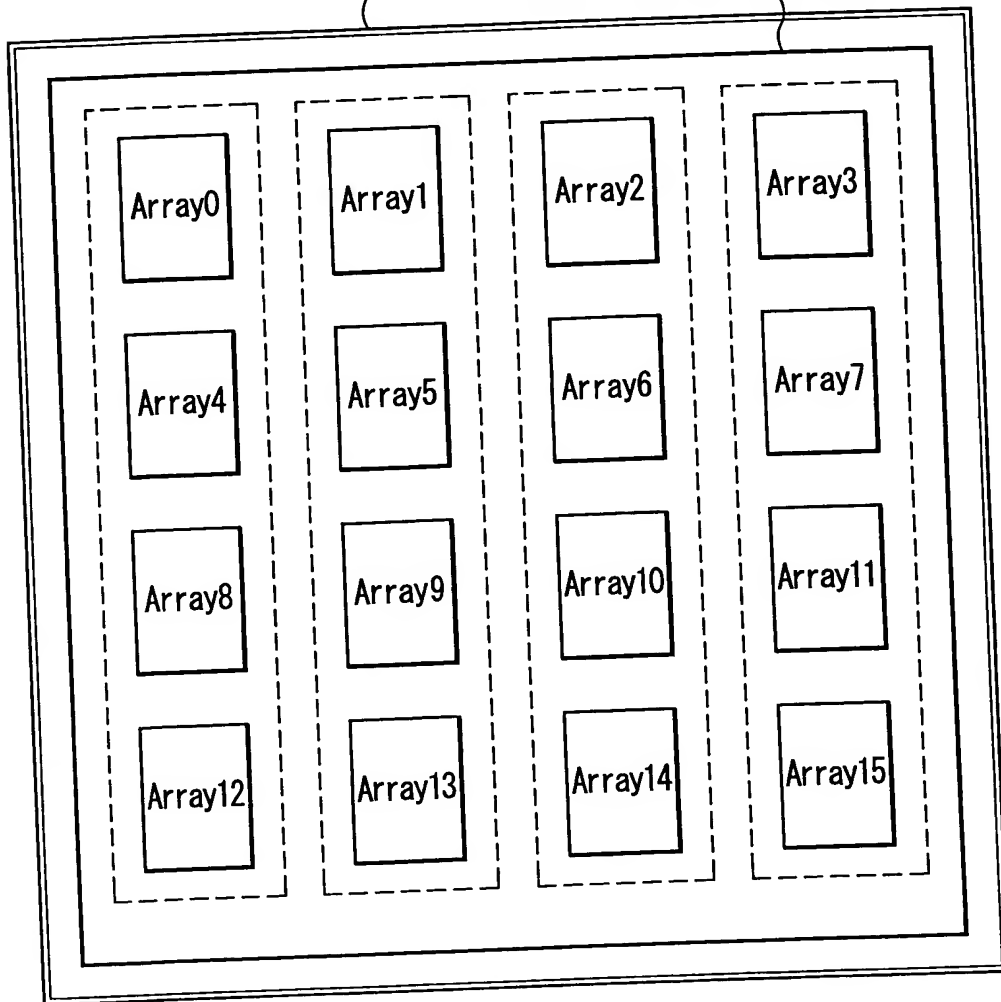


FIG. 12

4 Gbit package product  
(second generation product is used)

4 Gbit package product

2 Gbit(second generation) chip

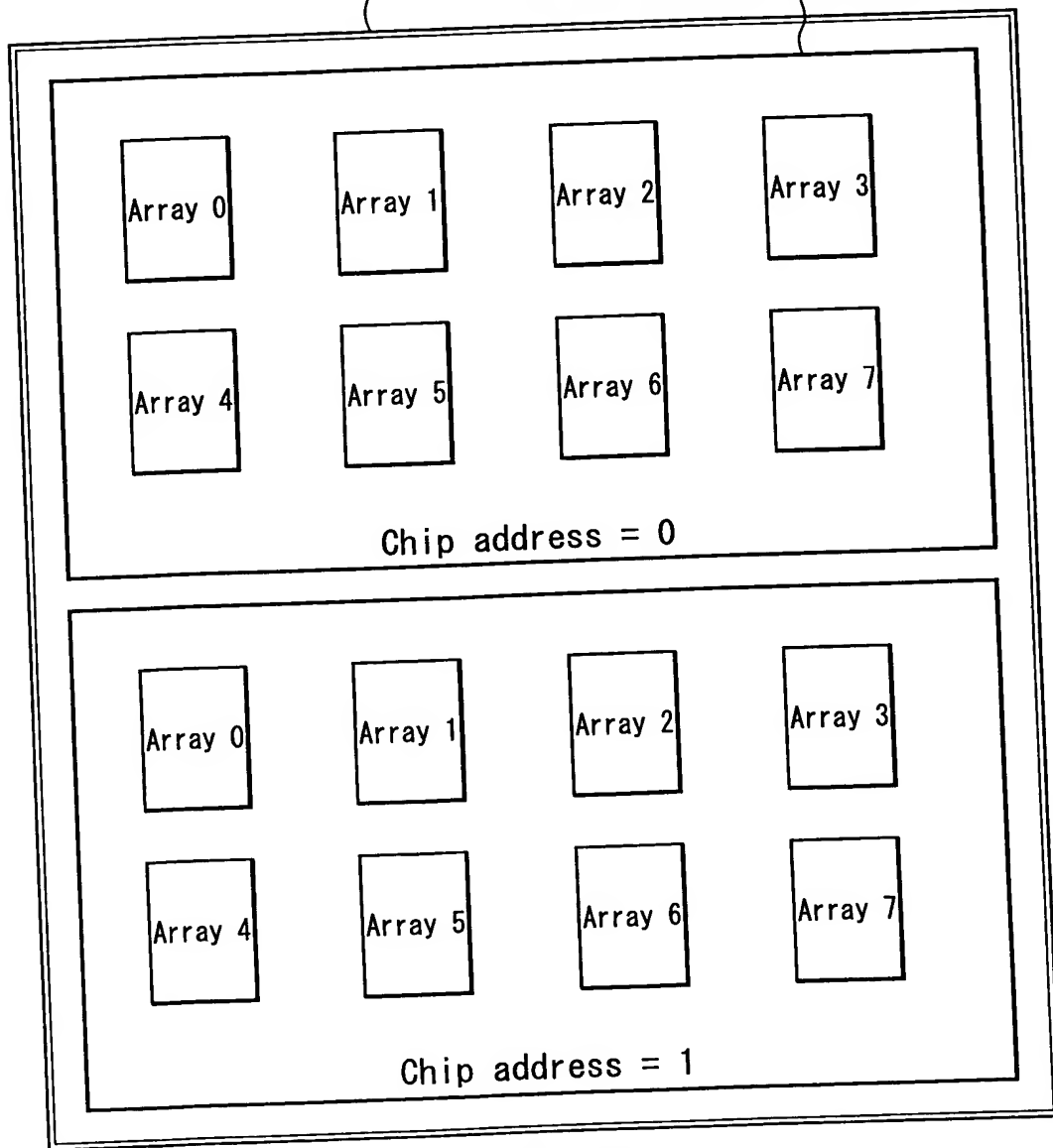


FIG. 13

Chip image when package product of FIG. 11 is seen from external device  
4 Gbit package product

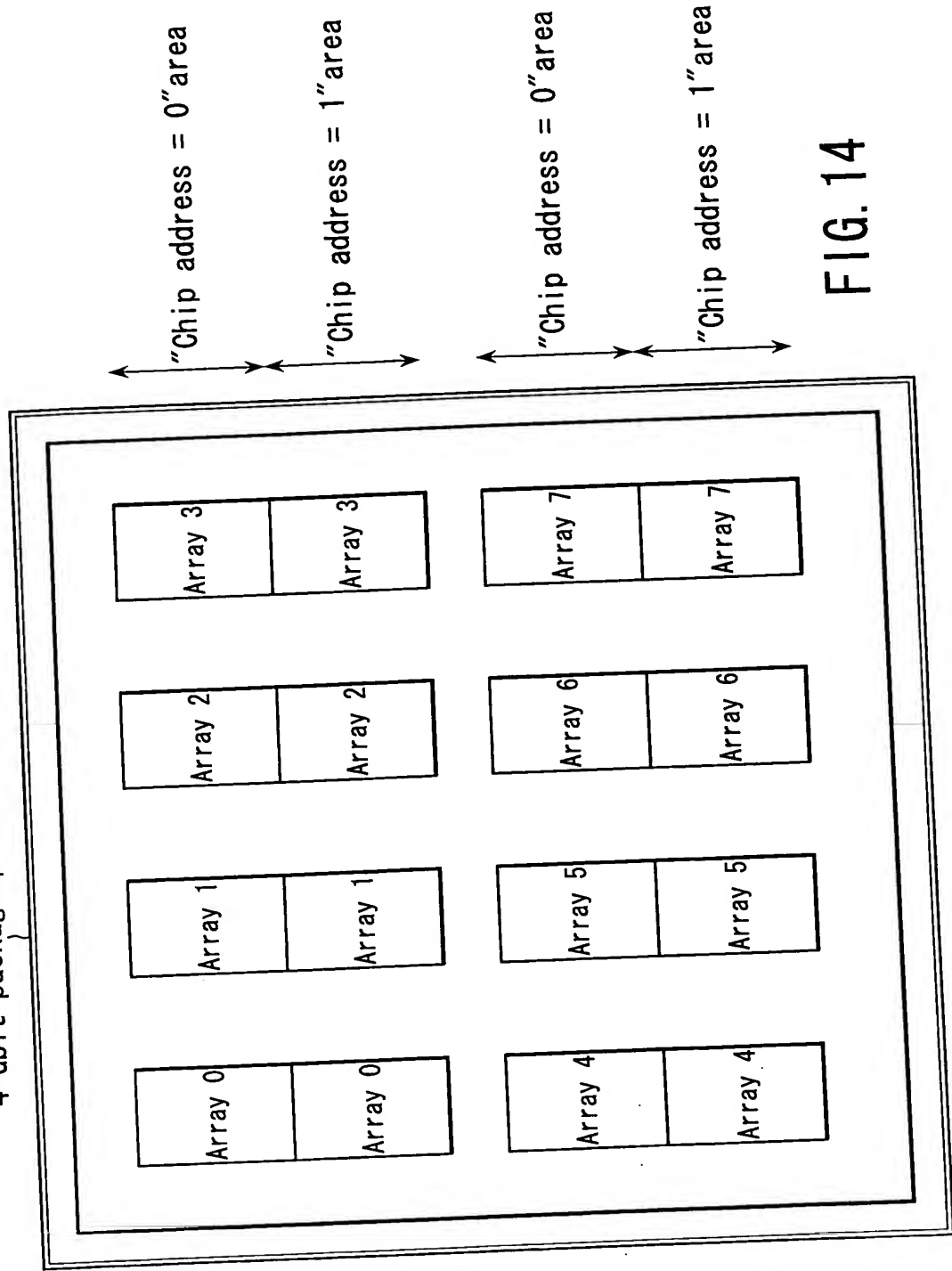


FIG. 14

4 Gbit package product (third generation product is used)  
Gbit package product  
4 Gbit (third generation) chip

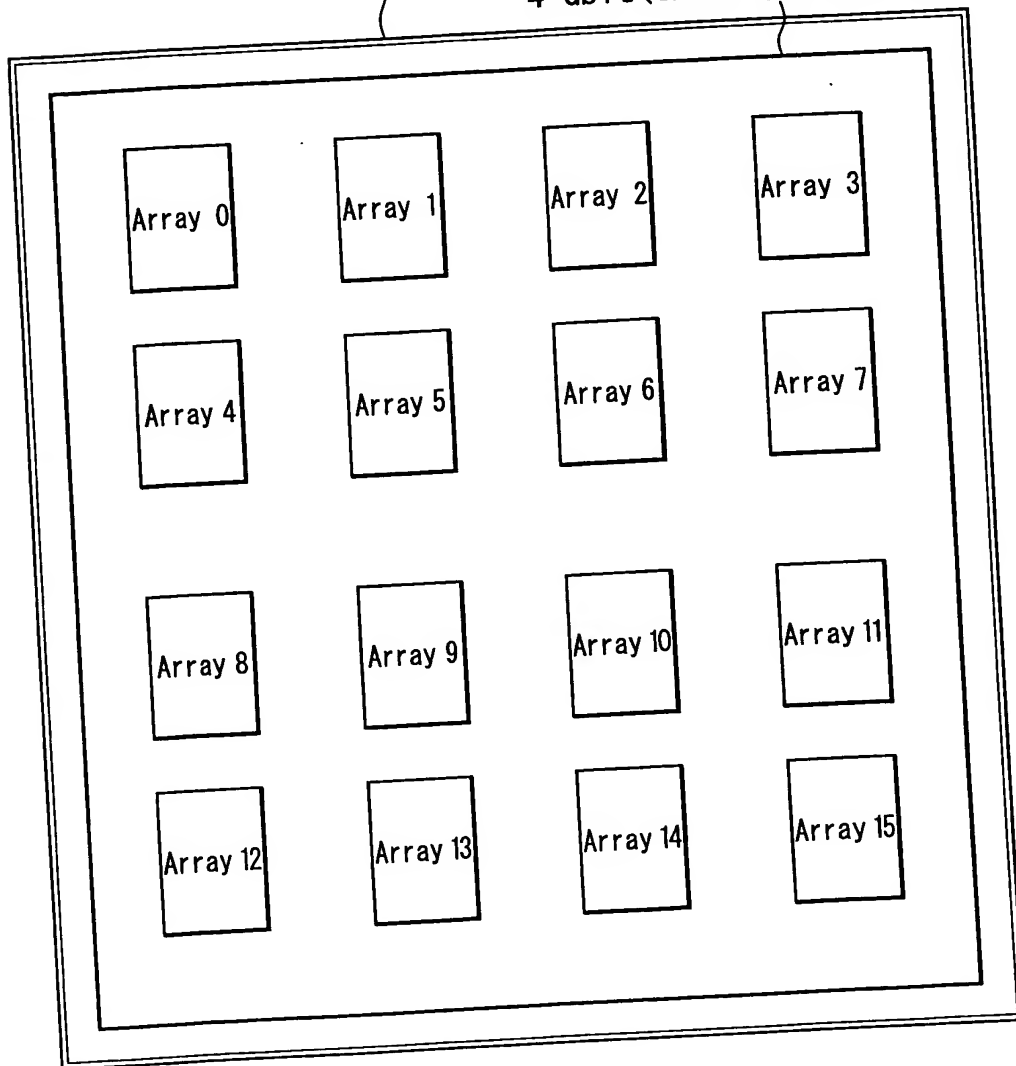


FIG. 15